A 1.9GHz Single-chip RF Front-end GaAs MMIC with Low-Distortion Cascode FET Mixer for Personal Handy-phone System Terminals

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ABSTRACT

This paper describes new shingle-chip RF front-end GaAs MMIC for 1.9GHz Japanese PHS handheld terminals. The IC consists of a high power amplifier, a T/R switch, a low noise amplifier, a newly developed low distortion cascode FET mixer and a negative voltage generator for FET gate bias voltage. The IC has high performance as RF front-end of terminals.

INTRODUCTION

With the recent worldwide progress in mobile personal communication system, the requirements for high performance, low power consumption and reducing size of handheld terminals and devices have been increased. These requirements has made the development of integration these circuits into a single chip [1], [2], [3], [4].

We have developed a highly integrated single-chip RF front-end GaAs MMIC for 1.9GHz Japanese Personal Handy-phone System (PHS), which consists of a high power amplifier (HPA), a T/R switch (SW), a low noise amplifier (LNA) and a newly developed low distortion cascode FET downconverter mixer (MIX).

The HPA is high efficiency (35%) and low distortion (Adjacent Channel leakage Power of –55dBc) with single DC voltage supply of +3V. A negative voltage generator (NVG) for FET gate bias is included in the IC.

The IC has high performance as receiver front-end for PHS terminals. Circuits of receiver front-end for PHS terminals should have low intermodulation distortion. In order to reduce total current as receiver front-end, a newly developed active cascode FET mixer has been employed. The mixer has high 3rd intercept point (IP3), high conversion gain with low current. The receiver section of the IC (SW-LNA-MIX chain) has noise figure of 3dB, conversion gain of 22.4dB, with consumption current of 4.6mA, and low distortion. It is equivalent to the best receiver front-end MMIC's for L-band personal communication currently available [5]. [6], [7], [8].

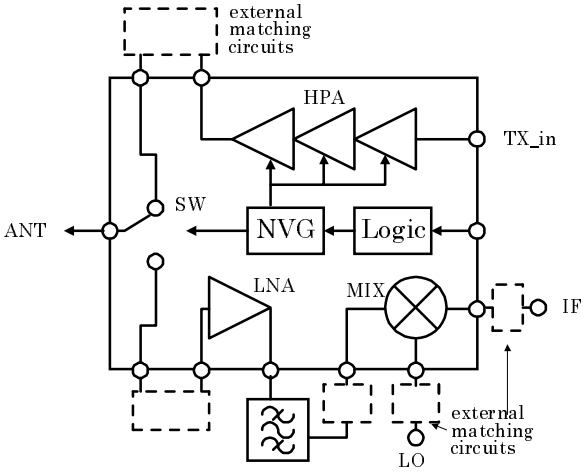

Fig.1 RF front-end MMIC for PHS

MMIC ARCHITECTURE

The architecture of the RF front-end MMIC for PHS terminals is shown in Figure 1. The IC consists of a high power amplifier (HPA), a SPDT T/R switch (SW), a low noise amplifier (LNA), a down converter mixer (MIX), a negative voltage generator (NVG) for HPA and SW gate bias, and logic circuits which controls above components. The IC needs single DC power supply of +3V.

Figure 2 shows a photograph of the MMIC. The E- and D-mode FET's are implemented as active device using an advanced SAG (Self-Aligned Gate) FET process technique [9]. In the IC, three kinds of

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threshold voltages for FET are adapted. The FET used in HPA and SW has high threshold voltage and break down voltage for high efficiency and high handling power. The FET for the LNA and the mixer has low threshold, which is used as D-mode FET in NVG and logic circuits. E-mode FET's with positive threshold voltage are used in NVG and logic circuits.

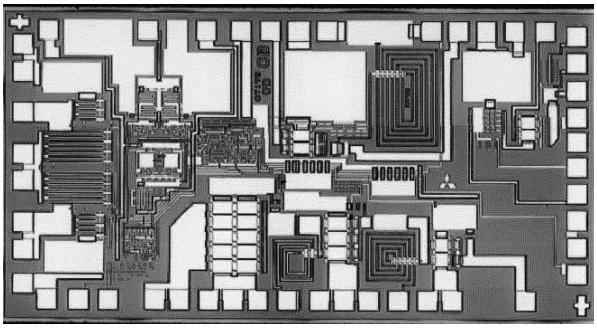

Fig. 2 Photograph of the MMIC

The design and measured performance of RF circuits is described below. Measurements have been done for the IC assembled in a 7mm x 6.4mm x 1.1mm (including pins) plastic package with 26pins. An exposed lead-frame at the bottom of the package achieves low ground inductance and reduces the number of pins for ground. The package has large contribution for miniaturizing.

HIGH POWER AMPLIFIER and T/R SWITCH

Figure 3 shows schematic for the high power amplifier. Dual gate FET's is used in driver stages (1st and 2nd stage) to achieve high gain with low consumption current. The output matching circuit is assembled outside the IC chip in order to reduce GaAs chip size and matching loss. Inter-stage matching circuits are consists of parallel inductors for drain bias circuits, and series capacitors for DC block. In order to reduce GaAs chip size, package leads have been employed as inductor for input and inter-stage matching circuits. Capacitors for DC bias are constructed outside of the package, thus no capacitor for bias circuits is on the chip. The load and source impedances for the final stage FET are determined for high efficiency with low distortion [10].

The RF leak power to the negative voltage generator from FET's of the HPA causes gate-bias voltage deviation due to the rectification effect in the generator circuit. To avoid this problem, a trap filter circuit for 1.9GHz has been employed between gates of FET and NVG. It consists of series resonant circuit of small capacitance and ground-terminated line. The ground-terminated line acts as isolation pattern between HPA and NVG/Logic circuits area [11].

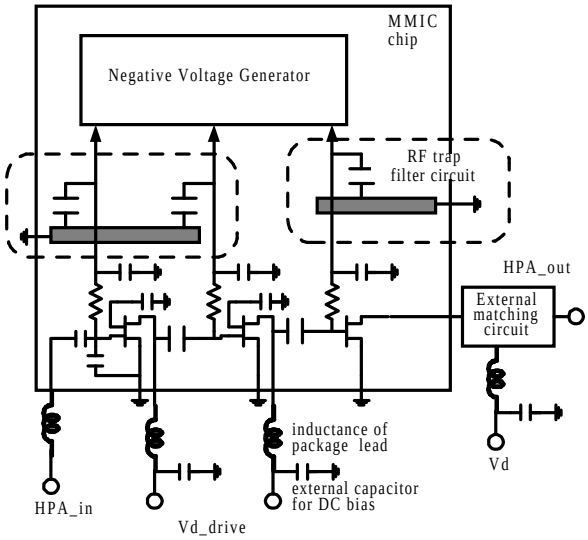

Fig. 3 Schematic for HPA

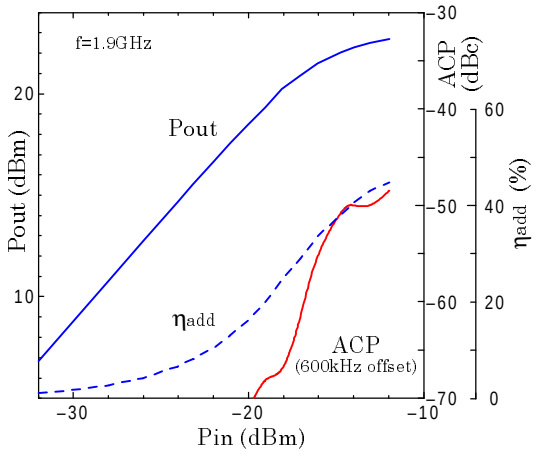

Fig. 4 Output power, ACP and efficiency for π/4 shift QPSK modulated signal

Figure 4 shows input-output power, ACP (Adjacent Channel leakage Power) and power added efficiency for π/4 shift QPSK. The HPA has output power of 21.5dBm with ACP of –55dBc and associate gain of 38dB. Power added efficiency of 35% has been obtained.

The T/R switch has SPDT configuration, which uses

series and shunt FET's. The drain and source of each FET is pulled up to +3V. At transmitting mode, negative voltage for gates of FET's is biased to have handling power of more than 22dBm. The same trap filter circuit, as mentioned in HPA section, is employed at gate bias circuit to suppress leakage of RF power to the NVG circuit.

The measured insertion loss at 1.9GHz is 0.6dB with an isolation of more 20dB. The handling power of more than 23dBm have been obtained.

LOW NOISE AMPLIFIER

The low noise amplifier consists of one-stage dual gate FET amplifier to achieve low consumption current and high gain simultaneously. An output matching circuit constructed in the chip, on the other hand, input matching circuit may be formed out of MMIC chip. A self-bias circuit is employed in LNA for single voltage operation without NVG. The consumption current of NVG is 3.2mA, which is comparable with the LNA and the mixer's consumption currents. Thus, NVG have to sleep during receiving mode for low power consumption. Moreover, influences for LNA caused by NVG noise can be avoid.

Figure 5 shows gain and NF of LNA at bias voltage of 3V and current of 2.3mA. The LNA has noise figure of 1.6dB, gain of 14dB and input 3rd intercept point (IIP3) of –6dBm has been obtained.

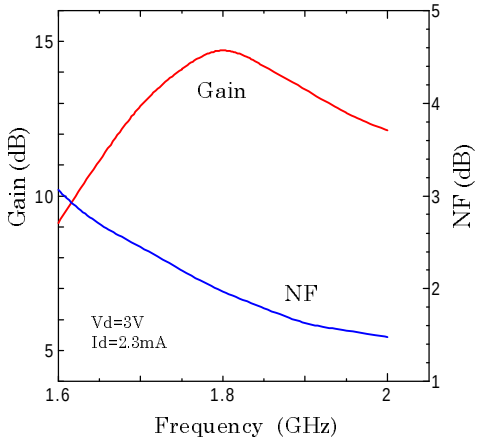

Fig. 5 Gain and NF of LNA

LOW DISTORTION CASCODE FET MIXER

The handheld terminals of PHS are also used as terminals of indoors digital cordless phone, thus components of the receiver should have low intermodulation distortion. The distortion of the mixer is more serious than the LNA, because amplified RF signals are applied to the mixer.

Passive (resistive) FET mixers have low intermodulation distortion, however, they have no conversion gain. Thus, LO and IF buffer amplifiers should be incorporated. These amplifier circuits occupy GaAs chip area and their consumption current can not be disregarded. Active dual gate FET (DGF) or cascode FET mixers do not have excellent intermodulation characteristics compared with passive mixers, however, these have large advantages of high conversion gain, low consumption current, small chip area because of single or two active devices, elimination of LO/RF diplexer or balun [12].

Table 1 Performance comparison of DGF mixer for LO injection port

LO injection Plo=-10dBm	1st gate	2nd gate
Gc	10dB	8dB
NF	7dB	9dB
IIP3	-8dBm	-2dBm

Table 2 Performance comparison of DGF and Cascode FET mixer

Plo=-10dBm	Dual Gate FET	Cascade FET
Gc	8dB	9dB
NF	9dB	7dB
IIP3	-2dBm	-2dBm
LO leakage	-20dBm	-20dBm

We have examined several configurations of DGF or cascode FET mixer to achieve low distortion characteristic. Comparison of DGF mixer performance for two configurations of LO injection into the 1st gate and the 2nd gate is shown in Table 1. A good results for input 3rd intercept point (IIP3) has been obtained with the configuration of 1st gate LO injection, however, the noise figure became worse. Then, we have compared 1st gate LO injection DGF mixer and 1st FET (lower FET) LO injection cascode FET mixer (Table 2). The noise figure is improved with cascode FET and there is no significant difference of LO leakage to RF port (2nd gate).

Figure 6 shows schematic of the mixer. LO power is injected into 1st FET (lower FET), RF signal is applied to the 2nd FET (upper FET) gate. A self-bias circuit is employed same as LNA. The gates of FET's are biased 0V with shunt inductors. The impedance of IF port circuit (drain circuit) have been optimized to realize high conversion gain and low distortion.

Figure 7 shows conversion gain, noise figure and

input 3rd intercept point (IIP3) versus LO power with bias voltage of 3V and current of 2.3mA. The conversion gain of 10dB, the noise figure of 6.5dB, and the IIP3 of –1dBm have been obtained with LO power of –10dBm. The IP3 performance is equivalent to passive or quasi-passive FET mixers as down converter for wireless communication terminals [6], [7].

When we put a bandpass filter with loss of 1dB between the LNA and the mixer, the performance of the IC as receiver front-end are NF of 3.0dB (at antenna terminal of T/R SW), conversion gain of 22.4dB with low consumption current (4.6mA) and low distortion (out IP3 at IF port is +9dBm).

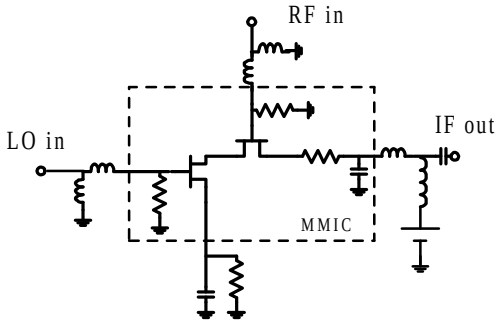

Fig. 6 Schematic for Mixer

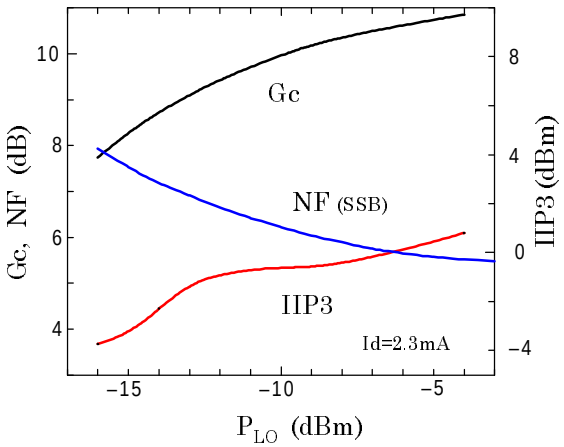

Fig. 7 Conversion gain, NF, and IIP3 of mixer

CONCLUSION

We have demonstrated the single-chip RF front-end GaAs MMIC for Japanese Personal Handy-phone System. It has high efficiency HPA, T/R switch, a LNA and a low-distortion down converter mixer. The IC employs a negative voltage generator for use of single voltage DC power supply. The HPA has an output power of 21.5dBm, with ACP of –55dBc and efficiency of 35%. The LNA has a noise figure of 1.6dB and a gain of 14dB with current of 2.3mA. The newly developed active cascode FET mixer has a high IIP3 of –1dBm with a high conversion gain of 10dB, low consumption current of 2.3mA. The IC has high performance for RF front-end of PHS handheld terminals. The IC is available in a 7.0mm x 6.4mm x 1.1mm plastic package.

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